Listing of Claims

1. (Previously Presented) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

a bias supply circuit for applying a voltage to said nonlinear device;

specific–frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal; and

an output terminal for outputting a signal.

2. (Previously Presented) A predistortion circuit of Claim 1, wherein said specific–frequency suppressing means has such impedance that the impedance of said specific–frequency suppressing means viewed from the connection point to which said specific–frequency suppressing means is connected is lower than the impedance of said nonlinear device viewed from said connection point at all or part of such frequencies that are from said frequency corresponding to DC to said frequency corresponding to said occupied band width.

3. (Previously Presented) A predistortion circuit of Claim 1 or 15, wherein said nonlinear device is provided between the connection point between said input terminal and said output terminal and the ground.

4. (Withdrawn) A predistortion circuit of Claim 1, wherein said nonlinear device is connected between said input terminal and said output terminal.

5. (Withdrawn) A predistortion circuit of Claim 1, wherein: said nonlinear device is a transistor; said input terminal is connected to any one of the drain and the source of the transistor; said output terminal is connected to the other of the drain and the source of said transistor; and said bias supply circuit is connected to the gate of said transistor.

6. (Previously Presented) A predistortion circuit of Claim 1 or 15, wherein said specific–frequency suppressing means comprises the all or part of a resistor, a coil, a capacitor, and a transmission line.

7. (Previously Presented) A predistortion circuit of Claim 1 or 15, wherein said nonlinear device comprises a diode.

8. (Withdrawn and Previously Presented) A predistortion circuit of Claim 1, wherein said nonlinear device comprises a transistor.

9. (Previously Presented) A power amplifier comprising: a predistortion circuit of Claim 1 or 15; and an amplifier for amplifying the signal from said predistortion circuit.

10. (Previously Presented) A power amplifier of Claim 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the gate of which is connected to said first matching circuit;

a second matching circuit connected to the drain of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific–frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

11. (Previously Presented) A power amplifier of Claim 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the base of which is connected to said first matching circuit;

a second matching circuit connected to the collector of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific–frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency

corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

12. (Previously Presented) A predistortion circuit of claim 1 or 15, wherein said specific–frequency suppressing means is composed of lumped parameter components interconnected in series.

13. (Previously Presented) A predistortion circuit of claim 6, wherein said specific–frequency suppressing means is composed of a transmission line.

14. (Previously Presented) A predistortion circuit of claim 6, wherein said specific–frequency suppressing means is composed of a transmission line and a capacitor interconnected in series.

15. (Previously Presented) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

a bias supply circuit for applying a voltage to said nonlinear device;

specific–frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device, said specific–frequency suppressing means suppressing at least one higher harmonic frequency of a carrier wave of said input signal; and

an output terminal for outputting a signal;

wherein said specific-frequency suppressing means has such impedance that the impedance of said specific-frequency suppressing means viewed from the connection point to which said specific-frequency suppressing means is connected is lower than the

impedance of said nonlinear device viewed from said connection point at said one higher harmonic frequency of a carrier wave of said input signal.

16. (Previously Presented) A predistortion circuit of Claim 15, wherein said one higher harmonic frequency is the second harmonic frequency.

17. (Previously Presented) A predistortion circuit of Claim 15, wherein said specific-frequency suppressing means is composed of lumped parameter components interconnected in series.

18. (Previously Presented) A predistortion circuit of Claim 15, wherein said specific-frequency suppressing means is composed of a transmission line.

19. (Previously Presented) A predistortion circuit of Claim 15, wherein said specific-frequency suppressing means is composed of a transmission line and a capacitor interconnected in series.